REMARKS

Claims 1-14 are pending in the application, with claims 3-6 and 9-12 having been withdrawn from consideration and claims 13-14 are added herein.

Claims 1-2 and 7-8 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the Applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated **January 3, 2003**.

As to the Examiner's outstanding objection to the Abstract of the Disclosure, as indicated above, the applicants have deleted the current Abstract, and submit herewith a substitute Abstract of the Disclosure in place therefor.

The Applicants respectfully request that the substitute Abstract of the Disclosure submitted herewith be approved by the Examiner.

Objection to the Specification

The Abstract has been objected to for having more than 150 words and for minor informalities.

The Abstract has been amended to reduce the number of words and to eliminate the informalities. This rejection is now considered to be moot.

Claim Rejections under 35 USC §112

Claim 7 is rejected under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 7 is supported by way of an example in Figure 17 and pages 74-75 of the written specification.

The requirement for making a burden of prove for a lack of enablement is specifically stated in MPEP 2164.04. From reviewing this section, it is the Applicants' understanding that to meet the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention, the Office should:

1. construe the claims and take position on terms that may lend multiple meaning;

2. provide a reasonable explanation as to why the scope of protection provided by a claim is not adequately enabled by the disclosure;

3. explain why the Office doubts the truth or accuracy of any statement in a supporting disclosure;

4. back up assertions of the Office with acceptable evidence or reasoning which is inconsistent with the contested statement; and

5. Give reasons for the uncertainty of the enablement.

Should the Office be unable to meet the requirement of these tests, then the Office has not met its initial burden in asserting a lack of enablement rejection. There would be no need for the applicant

to go to the trouble and expense of supporting his presumptively accurate disclosure.

Should the Office continue to maintain this rejection, explanations in compliance with MPEP 2164.04 are respectfully requested.

Claims 1-2 and 7-8 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1, as supported by Fig. 1 and pages 26-29 of the Specification, the Office Action states in paragraph 14, "the input signal goes through double invertors (1aa and 1ab in Fig. 1A). It is unclear how the inversion section outputs the inverted signal by inverting an inverted signal of the output signal".

The Office Action might have misunderstood that input signal (A) is inverted two times at invertors 1aa and 1ab. Namely, at first, inverter 1aa inverts input signal (A) and outputs thus inverted input signal (/A). Secondly, inverter lab inverts this 'inverted input signal (/A)' and outputs ' inverted inverted input signal (A)'.

Two CMOS logics 1aa and 1ab, however, are connected in parallel as supported by line 9, page 27 and line 1, page 28 in the Specification. The signal line P100 thus outputs the input signal and the inverted logic value as supported in lines 16-18, page 27 of the Specification.

Regarding Claim 7, as supported in line 9, page 76 to line 13, page 78 with Figs. 17, 18(a) and 18(b) and pages 74-76 of the Specification, the Applicant has clarified that 'the signal(s) being

switched' is (are) a signal (signals) inside the inversion sections. The signals inside the inversion sections are input S, XS, A1 and A2 as shown in Figs. 18(a) and 18(b) in paragraph 14.

However, note that **Freeman**, **Sung** and **Take** actually fail to teach a logic circuit.

Claim 7 (Fig. 17), as amended, calls for one of a leaf cells which form the carry generation circuit (Fig. 22), and including a logic circuit as amended claim 1.

Claim Rejections under 35 USC §102

Claim 1 is rejected under 35 USC §102(b) as being anticipated by Freeman (U.S. Re. 34,363).

Freeman merely discloses a configurable logic array comprising a plurality of configurable logic elements variably interconnected in response to control signals to perform a selected logic function. **Freeman** is totally silent about that claimed feature of the Applicant's invention.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Re claim 1, Freeman discloses in Figure 1 a logic circuit (22) comprising: a first inversion section (A) for inverting a first input signal having one of positive logic and negative logic and outputting the inverted signal; a second inversion section (B) for inverting a second input signal having the other the positive logic and the negative logic and outputting the inverted signal; and a transmission section (output C) for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable selection signal (SEL.) and an inverted signal of the selection signal. Basically, the present invention circuit is logic circuit that selectively outputting a signal from one of inputting inverted signals by the control signal. Freeman discloses in the specification that this logic circuit is called an inverting one of two inputs multiplexer (col. 4, line 29)."

The Office has essentially and cleverly copied the claim language of the present invention

and sparingly and selectively provided insertions alleging where the same element and feature is disclosed in the asserted prior art. However, the asserted prior art in fact does not substantiate the Office rejection because not each and every element is disclosed therein.

Specifically, it is a firm Office position that the asserted prior art discloses "a first inversion section (A) for inverting a first input signal having one of positive logic and negative logic and outputting the inverted signal." However, in reviewing relevant portion of Figure 1 of Freeman, there is no disclosure of outputting the inverted signal.

In contradistinction, in Figure 1 of the present invention, an inverted signal of A is indeed output from the first inversion section 1a as represented by the signal line P100.

It is well settled that:

> "A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

Should the Office continue to believe that the claimed invention is anticipated by the asserted prior art, a citation of where each and every claimed feature, either as column number and line number, or figure number and reference numeral, or a combination thereof, as disclosed in the asserted prior art is respectfully requested. Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

Claim Rejections under 35 USC §103

Claim 2 is rejected under 35 USC §103(a) as being obvious over Freeman (U.S. Re. 34,363) in view of Song (U.S. Patent No. 6,012,079).

Claim 2 is supported by way of an example in Fig. 2 and associated written Specification in pages 29-32.

Song merely discloses a sum adder, before carry propagation which is generated through multiplexer chain in respective sum generation blocks arrive at the final stage of the multiplexer chain, the final stage is driven by block carry signals BC_i and $/BC_i$ provided from the respective carry generation blocks. With this, an operation speed is improved, and the sum adder operates with low power consumption.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Freeman does not disclose the features of the second outputting section for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value, which depends upon an externally controllable second selection signal and an inverted signal of the second selection signal."

The Applicant agrees with this Office assessed shortcoming of Freeman. However, it should be noted that independent claim 2 also positively recited:

> " a first inversion section for inverting a first input signal and outputting the inverted signal;
>
> a second inversion section for inverting a second input signal and outputting the inverted signal".

These features are shown by way of an example in Figure 2, where there is indeed shown a first inversion section (2a) for inverting a first input signal (A1) and outputting the inverted signal (XA1); a second inversion section (2b) for inverting a second input signal (A2) and outputting the inverted signal (XA2).

The outstanding Office Action fails to show where these features are disclosed or taught in Freeman.

Therefore, even if **Freeman** and **Song** are combined, exactly as suggested in the outstanding Office Action, the claimed invention would not result. Therefore, claim 8 is not rendered obvious by the assert prior art.

Reconsideration and withdrawal of this rejection are respectfully requested.

Claim 8 is rejected under 35 USC §103(a) as being obvious over Freeman (U.S. Re. 34,363) in view of Taki (U.S. Patent No. 6,005,418).

Claim 8 is supported by way of an example in Figs. 1 and 20-21 and associated written Specification in pages 26-29 and 76-78.

Taki merely shows a low power consuming logic circuit (Fig. 3A), which restrains a short circuit current which flows in the CMOS inverter. With this, a consumed power can be reduced greatly.

Whereas in the applicant's process, unlike **Freeman**, **Song** and **Taki**, a transmission section selectively outputs the inverted first input signal or the inverted second input signal in accordance with a logical value which depends upon an externally controllable selection signal and an inverted signal of the selection signal.

Having been configured as such, the present logic circuit (LEOR; see Fig. 1) can operate at a high speed. Further, an isolation between a circuit following the transmission section and another circuit preceding to the logic circuit is strengthened. Furthermore, the logic circuit eliminates the necessity for providing a logic circuit in the circuit preceding to the logic circuit, also circuit configuration can be simplified.

In rejecting the claimed invention, the outstanding Office Action has specifically stated that:

> "Freeman does not disclose the first and second switching sections which capable of performing switching of whether the first and second input signals should be passed or blocked in accordance with an external control signal."

The Applicant agrees with the Office assessment of the shortcomings of **Freeman**.

The outstanding Office Action also stated that "Re claim 8, it has all the limitations in claim 1." The Applicants respectfully disagree. As also mentioned in the response to the rejection of claim 1, **Freeman** fails to disclose or teach the slightly amended feature of "a first inversion section (A) for inverting a first input signal having one of positive logic and negative logic and outputting an inverted first signal."

Therefore, even if **Freeman** and **Taki** are combined, exactly as suggested in the outstanding Office Action, the claimed invention would not result. Therefore, claim 8 is not rendered obvious by the assert prior art.

Reconsideration and withdrawal of this rejection are respectfully requested.

Prior Art Indicated To Be Pertinent To The Disclosure

The Office has provided a list of prior art indicated to be pertinent to the Applicant's invention. Consistent with the understanding as stipulated in MPEP 706.02 that only the best prior art should be applied, this list of prior art not having been applied by the Office, it is the Applicant's understanding that the Office must have considered the listed prior art to be no more pertinent than the applied prior art of record.

Conclusion

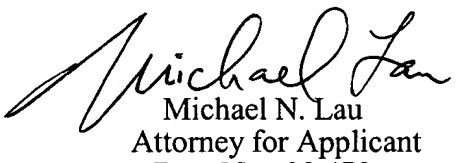
In view of the aforementioned amendments and accompanying remarks, all pending claims are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,
ARMSTRONG, WESTERMAN & HATTORI, LLP



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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made
Substitute Abstract of the Disclosure

Q:\FLOATERS\MLAU\000267\6-3-03 AMENDMENT

VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/522,470

IN THE CLAIMS:

Claims 1-2 and 7-8 have been amended to as follows:

1. **(Amended)** a logic circuit, comprising:

a first inversion section for inverting a first input signal having one of positive logic and negative logic and outputting an inverted first input [the inverted] signal;

a second inversion section for inverting a second input signal having the other of the positive logic and the negative logic and outputting an inverted second input [the inverted] signal; and

a transmission section for selectively outputting one of [the output] the inverted first input signal of said first inversion section and [the output] the inverted second input signal of said second inversion section in accordance with a logical value which depends upon an externally controllable selection signal and an inverted signal of the selection signal.

2. **(Amended)** A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;

a second inversion section for inverting a second input signal and outputting the inverted signal;

a first outputting section for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable first selection signal and an inverted signal of the first selection signal; and

a second outputting section for selectively outputting one of the output of said first inversion section and the output of said second inversion section in accordance with a logical value which depends upon an externally controllable second selection signal and an inverted signal of the second selection signal.

7. **(Amended)** A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;

a second inversion section for inverting the inverted signal of the first input signal and outputting a resulting signal;

a first outputting section for performing NANDing arithmetic between the output of said first inversion section and a second input signal and outputting a first resulting signal; and

a second outputting section for performing NANDing arithmetic between the output of said second inversion section and an inverted signal of the second input signal and outputting a second resulting signal;

said first outputting section and said second outputting section being switched with the

second input signal and the inverted signal of the second input signal, said first outputting section outputs the second resulting signal and said second outputting section outputs the first resulting signal.

8. **(Amended)** The logic circuit as claimed in claim 1, further comprising:

a first switching section provided on an input side of said first inversion section and capable of performing switching of whether the first input signal should be passed or blocked in accordance with an external control signal; and

a second switching section provided on an input side of said second inversion section and capable of performing switching of whether the second input signal should be passed OT blocked in accordance with the external control signal.